CLAIMS

What is claimed is:

1. A switching circuit comprising:

a first switching transistor having a control terminal coupled to a first input signal and having a first current carrying terminal;

a first current source coupled to the first current carrying terminal; and

a first isolation resistor connected in series between the first current carrying terminal and the current source, the isolation resistor reducing an in-rush current into a capacitance between the first isolation resistor and the current source to reduce distortion in an output signal of the circuit when the first switching transistor is switched.

2. The circuit of Claim 1 wherein the first switching transistor comprises an NPN bipolar transistor.

3. The circuit of Claim 1 wherein the first switching transistor comprises a MOSFET.

4. The circuit of Claim 1 wherein the first switching transistor forms part of a differential pair of switching transistors, the circuit further comprising:

a second switching transistor with a control terminal coupled to a second input signal and having a second current carrying terminal coupled to the first current carrying terminal of the first switching transistor.

5. The circuit of Claim 4 wherein the first switching transistor and the second switching transistor are bipolar transistors, and the first and second current carrying terminals are emitters of the first and second switching transistors.

6. The circuit of Claim 4 further comprising:

a second isolation resistor coupled in series between the first current carrying terminal of the first switching transistor and a second current carrying terminal of the second switching transistor; and

a second current source and a third isolation resistor in series between the second current carrying terminal and the second current source.

7. The circuit of Claim 6 wherein the first switching transistor and the second switching transistor are bipolar transistors.

8. The circuit of Claim 6 wherein the first switching transistor and the second switching transistors are MOSFET transistors.

9. A method of operation of a switching circuit, the switching circuit comprising a first switching transistor having a control terminal coupled to a first input signal and having a first current carrying terminal; a first current source coupled to the first current carrying terminal; and a first isolation resistor connected in series between the first current carrying terminal and the current source, the method comprising:

conducting a current through the isolation resistor during switching of the switching transistor to reduce an in-rush current into a capacitance between the first isolation resistor and the current source to reduce distortion in an output signal of the circuit when the first switching transistor is switched.

10. The method of Claim 9 wherein the first switching transistor comprises an NPN bipolar transistor.

11. The method of Claim 9 wherein the first switching transistor comprises a MOSFET.

12. The method of Claim 9 wherein the first switching transistor forms part of a differential pair of switching transistors, the circuit further comprising a second switching transistor with a control terminal coupled to a second input signal and having a second current carrying terminal coupled to the first current carrying terminal of the first switching transistor.

13. The method of Claim 12 wherein the first switching transistor and the second switching transistor are bipolar transistors, and the first and second current carrying terminals are emitters of the first and second switching transistors.

14. The method of Claim 12, the circuit further comprising a second isolation resistor coupled in series between the first current carrying terminal of the first switching transistor and a second current carrying terminal of the second switching transistor, wherein the first switching transistor and the second switching transistor are bipolar

transistors, and wherein the circuit further comprises a second current source and a third isolation resistor in series between the second current carrying terminal and the second current source, the method further comprising:

at least partially isolating effects of parasitic capacitances of the first switching transistor and the second switching transistor during switching by reducing transient current through the second isolation resistor flowing between the first switching transistor and second switching transistor; and

conducting a current through the third isolation resistor during switching of the second switching transistor to reduce an in-rush current into a capacitance between the third isolation resistor and the second current source to reduce distortion in an output signal of the circuit when the second switching transistor is switched.